What is claimed is:

1. A graphics system comprising:

generating logic for generating a mask identifying bits within a plurality of bits that are not to be impacted by a computation; and

compression logic responsive to the mask for generating a compressed bit stream, wherein the bits that are not to be impacted by the computation are not included in the compressed bit stream.

2. The system of claim 1, wherein the mask is a pixel mask corresponding to a tile of pixels to be displayed on a display.

3. The system of claim 1, wherein the generating logic is configured to generate the mask based on depth information.

4. The system of claim 3, wherein the depth information is obtained from a z-buffer.

5. The system of claim 1, wherein the compression logic comprises a plurality of multiplexers collectively configured to be capable of shifting individual bits of the plurality of bits by varying amounts based on the contents of the mask, wherein each additional shifted bits effectively overwrites bits that are to be unaffected by the computation.

6. The system of claim 5, further comprising compression control logic, the compression control logic configured to control the compression logic to shift individual bits by an amount equal to a number of bit positions, preceding the current bit position, that are unaffected by the computation.

7. The system of claim 1, further comprising decompression logic that decompresses compressed information, the decompression logic using the mask to decompress the information.

8. An apparatus for compressing a plurality of bits comprising:

a plurality of multiplexers arranged in a plurality of rows, wherein multiplexers in a first row have inputs connected to signals defining bits to be compressed and multiplexers of successive rows have inputs connected to outputs of the multiplexers of the preceding row, wherein each successive row of multiplexers comprises fewer multiplexers than the previous row; and

control logic for controlling data select input signals for the plurality of multiplexers such that individual bits of the plurality of bits are shifted varying amounts, the shift amount being determined by a mask.

9. The apparatus of claim 8, wherein the plurality of multiplexers are collectively configured to be capable of shifting individual bits of the plurality of bits by varying amounts based on the contents of the mask, wherein each additional shift value effectively causes a shifted bit to overwrite a bit that is to be unaffected by a subsequent computation.

10. The apparatus of claim 9, further comprising compression control logic, the compression control logic configured to control the control logic to shift individual bits by an amount equal to a number of bit positions, preceding the current bit position, that are to be unaffected by the computation.

11. The apparatus of claim 8, wherein the mask is a pixel mask corresponding to a tile of pixels to be displayed on a display.

12. The apparatus of claim 11, wherein contents of the pixel mask are based on depth information.

13. The system of claim 8, wherein groups of the plurality of bits define data values representing an attribute for pixels to be displayed on a display.

14. The system of claim 13, wherein the attribute is one selected from the group consisting R, G, B, A, U, and V.

15. A component for a computer graphics system comprising logic for compressing a plurality of groups of bits based on a pixel mask, wherein contents of the pixel mask are derived by a determination of corresponding groups of bits that are to be unaffected by a computation, the contents of the pixel mask defining variable amounts that the plurality of bits are shifted during the compression.

16. The component of claim 15, wherein each position of the pixel mask defines a shift amount for a group of bits.

17. The component of claim 16, wherein the content of each position of the pixel mask is defined by a single bit, and the shift amount for a group of bits is defined by a summation of preceding pixel mask positions whose contents indicate corresponding pixels are not to be affected by a subsequent computation, wherein the positions of the pixel mask are arranged in an order and the preceding pixel mask positions are those that, as ordered, numerically precede the a given position.

18. The component of claim 17, wherein the arranged order of the pixel positions of the pixel mask is arbitrary.

19. A computer graphics system comprising:

logic for compressing a plurality of groups of bits to eliminate groups of bits that are to be unaffected by a computation;

logic for performing the computation;

logic for decompressing corresponding data after performing the computation to restore data corresponding to previously eliminated groups of bits.

20. The computer graphics system of claim 19, wherein the logic for performing the computation comprises a multi-threaded processing unit.

21. The computer graphics system of claim 20, wherein computation is a pixel shading operation.

22. A graphics system comprising:

mask logic for generating a mask identifying positions within a plurality of positions of a bit stream that are to be removed during a compression operation; and

compressing logic responsive to the mask for generating a compressed bit stream, wherein the positions that to be removed are removed by variably shifting contents of successive positions by an appropriate amount so as to overwrite contents of positions that are to be are to be removed.

23. The system of claim 22, wherein the mask is a pixel mask corresponding to a tile of pixels to be displayed on a display.

24. The system of claim 22, wherein the mask logic is configured to generate the mask based on depth information.

25. The system of claim 24, wherein the depth information is obtained from a z-buffer.

26. The system of claim 22, wherein the compressing logic comprises a plurality of multiplexers collectively configured to be capable of shifting individual bits of the bitstream by varying amounts based on the contents of the mask, wherein each additional shifted bits effectively overwrites bits that are to be unaffected by the computation.

27. The system of claim 26, further comprising compressing control logic, the compressing control logic configured to control the compressing logic to shift individual bits by an amount equal to a number of bit positions, preceding the current bit position, that are to be removed.

28. An apparatus for compressing a plurality of bits comprising:

a plurality of multiplexers arranged in a plurality of rows, wherein multiplexers in a first row have inputs connected to plurality of signals, some of which are to be removed through compression, and multiplexers of successive rows have inputs connected to outputs of the multiplexers of the preceding row;

control logic for controlling data select input signals for the plurality of multiplexers, the control logic being responsive to a mask that defines positions of the plurality of signals as the inputs of the first row of multiplexers that are to be removed through compression, such that input signals following input signals that are to be removed are shifted into the position of the preceding signals that are to be removed.

29. The apparatus of claim 28, wherein the plurality of multiplexers are collectively configured to be capable of shifting individual signals of the plurality of input signals by varying amounts based on the contents of the mask, wherein each additional shift value effectively causes a shifted bit to overwrite a signal position that is to be removed.

30. The apparatus of claim 29, further comprising compression control logic, the compression control logic configured to control the control logic to shift individual signals by an amount equal to a number of signal positions, preceding the current signal position, that are to be removed.

31. A component for a computer graphics system comprising logic for compressing a plurality of groups of bits by shifting compressed groups of bits into bit positions that are to be removed during the compression, the logic being responsive to a mask, wherein contents of the mask define variable amounts that the plurality of bits are shifted during the compression.

32. The component of claim 31, wherein the mask is a pixel mask and the groups of bits to be compressed correspond to attributes associated with pixels to be displayed.

33. The component of claim 31, wherein each position of the mask defines a shift amount for a group of bits.

34. The component of claim 33, wherein the content of each position of the mask is a defined by a single bit, and the shift amount for a group of bits is defined by a summation of preceding mask positions whose contents indicate corresponding pixels are not to be affected by a subsequent computation, wherein the positions of the mask are arranged in an order and the preceding mask positions are those that, as ordered, numerically precede the a given position.

35. The component of claim 34, wherein the arranged order of the positions of the mask is arbitrary.